Notice of Allowability	Application No.	Applicant(s)	
	09/704,529	MAEJIMA ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address*--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filing dated 05/09/07*.

2. ☒ The allowed claim(s) is/are *45-53*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____

Long Pham
Primary Examiner
Art Unit: 2814

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Ronald Shore on 09/28/07.

The application has been amended as follows:

45. (currently amended) A process for producing a semiconductor device, consisting essentially of:

providing a wafer for forming an integrated circuit thereon, the wafer having a main surface on which an integrated circuit is to be formed, a substantially circular contour portion surrounding said main surface, a curved positioning notch formed in said circular contour portion and connecting portions defined between said circular contour portion and said curved positioning notch;

wherein an outer peripheral part of said wafer is chamfered in a thickness direction by mechanical chamfering, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by mechanical chamfering.

46. (currently amended) A process for producing a semiconductor device, consisting essentially of:

providing wafer for forming an integrated circuit thereon, the wafer having a main surface on which an integrated circuit is to be formed, a substantially circular contour portion surrounding said main surface, a curved positioning notch formed in said circular contour portion and connecting portions defined between said circular contour portion and said curved positioning notch;

wherein an outer peripheral part of said wafer is chamfered in a thickness direction by grindstone, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by grindstone.

47. (currently amended) A process for producing a semiconductor device, consisting essentially of:

providing a wafer for forming an integrated circuit thereon, the wafer having a main surface on which an integrated circuit is to be formed, a substantially circular contour portion surrounding said main surface, a curved positioning notch formed in said circular contour portion and connecting portions defined between said circular portion and said curved positioning notch, wherein said connecting portions are chamfered in a plane parallel to said main surface; and

positioning said wafer by rotating said wafer.

48. (previously presented) A process for producing a semiconductor device according to claim 47, wherein, in the positioning step, positioning said wafer by using photoelectric elements.

49. (previously presented) A process for producing a semiconductor device according to claim 48, wherein an outer peripheral part of said wafer is chamfered in a thickness direction by mechanical chamfering, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by mechanical chamfering.

50. (previously presented) A process for producing a semiconductor device according to claim 48, wherein an outer peripheral part of said wafer is chamfered in a thickness direction by grindstone, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by grindstone.

51. (previously presented) A process for producing a semiconductor device according to claim 47, wherein, in the positioning step, positioning said wafer by optical means.

52. (previously presented) A process for producing a semiconductor device according to claim 47, wherein an outer peripheral part of said wafer is chamfered in a thickness direction by mechanical chamfering, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by mechanical chamfering.

53. (previously presented) A process for producing a semiconductor device according to claim 47, wherein an outer peripheral part of said wafer is chamfered in a thickness direction by grindstone, and

wherein said connecting portions are chamfered in a plane parallel to said main surface by grindstone.

54-60. (cancelled)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

/L. P./